METHOD AND APPARATUS FOR TRIMMING INTEGRATED CIRCUITS

CROSS-REFERENCE TO RELATED APPLICATION(S)

None.

BACKGROUND OF THE INVENTION

The invention relates to the trimming of integrated circuits. In particular, the invention relates to the trimming of integrated circuits using fuse circuitry, while minimizing the amount of die area consumed by the fuse circuitry.

During the manufacturing of integrated circuits, process variations can result in variations in electrical characteristics of the circuitry. A technique known as trimming is typically used to compensate for process variations. After the circuit manufacturing, various components of the integrated circuit are adjusted, or trimmed, to bring the electrical characteristics within permitted parameters. For example, trimming can be used to adjust resistances or capacitances, to adjust transconductance values, and to correct for DC offsets produced by process variations.

One trimming technique makes use of fuse circuitry, which is incorporated into the integrated circuit. Based upon a functional measurement of the integrated circuit performed by probing the wafer during an initial wafer test, the need for trimming is identified. Selected fuses are then blown to make the necessary adjustments to the integrated circuit.

Fuse circuits used for device trimming require fuse probe pads and wide metal lines to accommodate the large currents which are necessary for fuse blowing. The large physical size of these fuse components, compared to their simple function, contributes disproportionally to the die size. This is undesirable because the fuse components take up a significant amount of die area that could otherwise be allocated to other useful circuits, or allow a smaller die to be used.

In an attempt to counteract this disproportionate use of die area by fuse circuitry, design rules have attempted to compact the fuse circuitry, and the number of fuses used in an integrated circuit is typically limited. However, fuse

component sizes and the associated design rules still dictate large die area usage, and minimizing the number of trim fuses hampers a designer's ability to assign the optimum number of trim circuits.

BRIEF SUMMARY OF THE INVENTION

An integrated circuit wafer with significant savings in integrated circuit die area is achieved by positioning fuse circuits (fuses and associated circuitry) adjacent to the scribe lane between integrated circuits, and locating the fuse pads and power supply pads within the scribe lane. Conductors extend from the fuse circuits within the integrated circuit into the scribe lane to connect the pads to the fuse circuit. When the integrated circuits are severed from the wafer, the pads located within the scribe lane are severed from the integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an on-die fuse cell of the present invention with fuse pads located in adjacent scribe lane.

Figure 2 is an enlarged view of a portion of the fuse cell of Figure 1.

Figure 3 shows the fuse cell of Figure 1 after the die has been severed from the wafer.

DETAILED DESCRIPTION

Figure 1 shows a portion of integrated circuit wafer 10, on which integrated circuits are formed. Scribe lanes 14 separate integrated circuits 12 from one another, and provide an area in which scribing occurs to separate the individual integrated circuit die 12 from wafer 10.

Figure 1 illustrates on-die fuse cell 20 which is configured in accordance with the present invention. Fuse cell 20 includes five fuses 22A, 22B, 22C, 22D, and 22E which are oriented along die edge 24.

Connected to one end of each fuse 22A-22E are fuse pads 26A-26E and fuse circuitry 28A-28E, respectively. A power supply pad is connected to an

opposite side of each fuse. Power supply pad 30 is connected to fuses 28A and 28B. Power supply pad 32 is connected to fuses 22C and 22D. Supply pad 34 is connected to fuse 22E.

Fuses 22A-22E are oriented parallel to die edge 24 and are immediately adjacent to scribe lane 14. Fuse circuitry 28A-28E is also positioned as close as possible to die edge 24. The location and orientation of fuses 22A-22E and fuse circuitry 28A-28E minimizes their intrusion into die 12. This minimizes their area usage and avoids interference with other on-chip circuitry as much as possible.

Further on-die space is saved by positioning fuse pads 26A-26E and power supply pads 30, 32, and 34 in scribe lane 14. These pads are used only during the fuse blowing process, which occurs after wafer test and before the individual integrated circuit die 12 is severed from wafer 10. Once the fuse is blown, pads 26A-26E, 30, 32, and 34 are no longer needed. They become sacrificial, since they are located in the scribe lane. Having performed their task prior to wafer dicing, they are no longer needed and are removed when the scribe lanes are cut.

Also shown in Figure 1 is supply bus 36. The remaining circuitry on integrated circuit die 12 is not shown. Also, the connection of fuse circuitry 28A-28E to the remaining circuitry of integrated circuit 12 is not shown.

During the wafer test, each integrated circuit is individually tested. Based upon those tests, selected fuses are blown by applying electrical current through the appropriate fuse and supply pads. For example, if fuse 22B were to be blown, current would be supplied through probes and connect with supply pad 30 and fuse pad 26B to cause fuse 22B to be blown.

During normal operation of the integrated circuit, fuse circuitry 28A-28E detect the fuse states (connected or blown) of their associated fuses 22A-22E

respectively, and provide appropriate signals to the circuitry of integrated circuit 12 based upon those fuse states.

Figure 2 is an enlarged view of a portion of Figure 1. In particular, fuse 22E is shown in more detail. Fuse 22E is typical of each of the fuses 22A-22E shown in Figure 1.

As seen in Figure 2, fuse 22E includes fuse element 40 which is positioned between conductors 42 and 44. Conductor 42 is connected to fuse circuitry 28E. In addition, conductor 42 is connected to fuse pad 26E by conductor 46.

Conductor 44 is connected by conductor 48 to supply pad 34 and by conductor 50 to supply bus 36. Supply bus 36 provides the supply signal to the fuses after the supply pads adjacent to the fuses have been cut away (see Figure 3). Conductors 46 and 48 extend from scribe lane 14 across die edge 24 to conductors 42 and 44, respectively. After wafer dicing, conductors 46 and 48 are severed so that only a remnant stub remains. This is seen along the right edge of Figure 3.

Figure 3 shows wafer 12 and fuse cell 20 after integrated circuit die 10 has been severed from wafer 10. Pads 26-26E, 30, 32, and 34 have be removed as part of the severing process, and do not occupy die area. Severed edges 60 are created by the severing process, and are close to die edges 24.

Another important advantage of the fuse cell of the present invention is the use of fuse and supply pads which are contacted only by probes during the fuse blowing process. None of the pads later function as bond pads, as has been the case in prior art on-die fuse cells. Since none of the fuse pads are bonded, an associated electrostatic discharge (ESD) protection device is not required in association with each fuse. This also results in a significant saving in the die area occupied by the fuse cell.

By minimizing the area occupied on the integrated circuit die by the fuses and their associated pads and circuitry, significantly less die area is consumed

by the on-die fuse cell. As a result, a larger percentage of the die is available for other on-chip circuitry. Also, because the on-chip impact of each fuse is significantly reduced, additional fuses desired by designer can be accommodated with minimal impact to die size.

Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention. For example, this invention is not limited to a fuse connection to a supply pad. Fuses can be connected to a positive supply, a negative supply, ground, or any other signal. It is not necessary that a common signal be used for all of the fuses on an integrated circuit. Each fuse could be connected to a dedicated pair of pads that connect to nothing other than the fuse and the associated fuse sensing circuitry.